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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/433,654	11/03/1999	JASMIN AJANOVIC	042390.P6740	2822

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EXAMINER	
STEVENS, ROBERTA A	

ART UNIT	PAPER NUMBER
2665	16

DATE MAILED: 06/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/433,654	AJANOVIC ET AL.	
	Examiner	Art Unit	
	Roberta A Stevens	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *33-69* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *33,35-38, 40, 42-44, 46, 49, 52, 54-56, 58, 59, 61, 62, 64, 66 and 68* is/are rejected.

7)☒ Claim(s) *34,39,41,45,47,48,50,51,53,57,60,63,65,67 and 69* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *13*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 33, 37, 40, 46 and 66 are rejected under 35 U.S.C. 102(e) as being anticipated by Ellis (U.S. 6191713 B1).

3. Regarding claim 33, Ellis teaches (figure 1) a system comprising: a process (110); a processor bus (115) coupled to the processor; a memory (135); a memory control hub (120) coupled to the processor bus and coupled to the memory; a graphic accelerator (125) coupled to the memory control hub; a bus (140) coupled to the memory control hub, to transmit packets; an input-output device (150); and an input-output hub (145) coupled to the bus and to the input-output device, wherein the system is capable of passing messages between the memory control hub and the input-output hub through packets transmitted on the bus, the messages including information about signals received from one or more of the processor, the memory, and the input-output device (col. 3, lines 1-56).

4. Regarding claim 37, Ellis teaches (col. 4, line 44 - col. 5, line 51) control information for the bus is embedded in the packet.

5. Regarding claim 40, Ellis teaches (figure 1) a chipset comprising: a memory control hub (120) capable of being coupled with a processor (110) and capable of being coupled with a memory (135); a bus (140) coupled to the memory control hub, to transmit packets; and an input-output hub (145) coupled to the bus and capable of being coupled to a input-output device, wherein the chipset is capable of passing messages between the memory control hub and the input-output hub through packets transmitted on the bus, the messages including information about signals (col. 4, line 44 – col. 5, line 51) received from one or more of the processor, the memory, and the input-output device (col. 3, lines 1-56).

6. Regarding claim 46, Ellis teaches (figure 1) a system comprising: a first hub (120) to receive a first signal; a first hub interface (140) coupled to the hub, to receive a message that is passed from the first hub, the message corresponding to the first signal, including a packet including control information (col. 4, line 44 – col. 5, line 51); a second hub (145) coupled to the first hub interface, to receive the message from the fist hub interface (col. 3, lines 1-56).

7. Regarding claim 66, Ellis teaches (col. 3, lines 1-56) a method comprising: receiving a first signal at a first hub coupled to a hub interface; passing a message corresponding to the first signal from the first hub through the first hub interface, the message including a packet including control information (col. 4, line 44 – col. 5, line 51); and receiving the message from the hub interface at a second hub coupled to the hub interface.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

10. Claims 35, 36, 42, 43, 49, 52, 54, 55, 58, 62, 64 and 68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ellis in view of the admitted prior art.

11. Regarding claims 35, 42, 49 and 54, Ellis does not teach packets comprising special cycle encoding a command to assert a PHLD signal.

12. The admitted prior art teaches that PHLD signals are well known in the art . Therefore it would have been obvious to one of ordinary skill in this art to adapt PHLD signals to Ellis' system as they are well known in the art.

13. Regarding claims 36, 43 and 55, Ellis does not teach packets comprising special cycle encoding a command to act as if SERR# was received.

14. The admitted prior art teaches that SERR# signals are well known in the art in the implementation o PCI bus. Therefore it would have been obvious to one of ordinary skill in this art to adapt SERR# signals to Ellis' system as they are well known in the art.

15. Regarding claim 52, Ellis teaches (figure 1) an apparatus comprising: a first component (120); a bus (140) coupled to the first component, to transmit packets; and a second component (145) coupled to the bus to receive the packets from the first component via the bus.

16. Ellis does not teach packets including special cycle packets embodying control information.

17. The admitted prior art teaches that packets including special cycle packets embodying control signals are well known in the art in the implementation o PCI bus. Therefore it would have been obvious to one of ordinary skill in this art to adapt such signals to Ellis' system as they are well known in the art.

18. Regarding claim 58, Ellis teaches (figure 1) the first component comprises a memory control hub (120), and the second component comprises an input-output hub (145).

19. Regarding claim 62, Ellis teaches (col. 3, lines 1-56) a method comprising: receiving a signal at a fist component; passing a first message that encodes information relevant to the signal

from the first component through a bus coupled to the first component; and receiving the first message from the bus at a second component.

20. Ellis does not teach packets including special cycle packets including control information.

21. The admitted prior art teaches that packets including special cycle packets embodying control signals are well known in the art in the implementation o PCI bus. Therefore it would have been obvious to one of ordinary skill in this art to adapt such signals to Ellis' system as they are well known in the art.

22. Regarding claims 64 and 68, Ellis does not teach packets including special cycle packets embodying control information.

23. The admitted prior art teaches that packets including special cycle packets embodying control signals are well known in the art in the implementation o PCI bus. Therefore it would have been obvious to one of ordinary skill in this art to adapt such signals to Ellis' system as they are well known in the art.

24. Claim 59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ellis in view of the admitted prior art and further in view of Olarig (U.S. 6009524(.

25. Regarding claim 59, Ellis teaches (figure 1) a graphics accelerator (125) and a memory (135) coupled to the first component.

26. Ellis does not teach FLASH bios coupled to the second component.

27. Olarig teaches (abstract) FLASH bios. It would have been obvious to one of ordinary skill in the art to adapt to Ellis and the admitted prior art Olarig's FLASH bois to store and protect personal information.

28. Claims 38, 44, 56 and 61 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ellis in view of Popat (U.S. 5564114).

29. Regarding claims 37, 44, 56 and 61, Ellis does not teach split-transaction protocol.

30. Popat teaches (col. 6, lines 9-12) split-transaction protocol. It would have been obvious to one of ordinary skill in this art to adapt to Ellis' system Popat's teachings of split-transaction protocol to free up the bus for use by other devices during data retrieval.

Allowable Subject Matter

31. Claims 34, 39, 41, 45, 47, 48, 50, 51, 53, 57, 60, 63, 65, 67, and 69 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

32. Any inquiry concerning the communication or earlier communications from the examiner should be directed to Roberta Stevens whose telephone number is *(703) 308-6607*. The examiner can normally be reached on Monday through Friday from 9:00 am to 5:30 p.m.

33. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor can be reached on *(703) 308-6602*.

34. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the group receptionist whose telephone number is *(703) 305-3900.*

35. **Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to: (703) 872-9306

For informal draft communications, please label "PROPOSED" or "DRAFT"

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA. Sixth Floor (Receptionist).

Roberta A. Stevens

Patent Examiner

05-27-04

STEVEN NGUYEN
PRIMARY EXAMINER